Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-76. (Canceled)

77. (Currently Amended) A method of forming a patterned layer during manufacture of an integrated circuit, comprising:

selectively irradiating with at least one type of radiant energy portions of a surface of a layer by electronically controlling individually each of a plurality of exposure elements; and

performing chemical processing of the surface including irradiated portions thereof to produce the patterned layer.

78. (Previously Presented) The method of claim 77, wherein the type of radiant energy is selected from the group consisting of optical, X-ray, E-beam and particle beam.

79. (Previously Presented) The method of claim 77, wherein the exposure elements are miniature sources of at least one of the following types of radiant energy: X-ray, Deep Ultra Violet and E-beam.

80. (Previously Presented) The method of claim 77, wherein the exposure elements control passage of radiant energy from an external source.

81. (Previously Presented) The method of claim 80, wherein the exposure elements control passage of radiant energy from an external source using at least one of the following mechanisms: electromagnetic deflection, electrostatic deflection and mechanical shuttering.

82. (Previously Presented) The method of claim 77, wherein chemical processing comprises etching.

83. (Previously Presented) The method of claim 77, wherein chemical processing comprises radiation-induced chemical vapor deposition.

84. (Previously Presented) The method of claim 77, further comprising separately focusing radiant energy emitted from the plurality of exposure elements.

85. (Previously Presented) The method of claim 77, further comprising:

ceasing irradiating the surface;

shifting the plurality of exposure elements with respect to the surface; and

resuming irradiating the surface.

86. (Currently Amended) A semiconductor processing lithography apparatus for maskless pattern generation comprising:

an array of radiation source cells arranged in rows and columns, the array being formed on a substrate; <u>and</u>

control logic integrated with the substrate for individually controlling each cell, wherein each cell comprises:

an exposure source; and

an aperture through which the exposure source emissions pass onto a surface to be exposed.

87. (Currently Amended) The apparatus of claim 86, wherein ~~the~~ each radiation source ~~cells expose~~ <u>cell exposes</u> separate areas of the surface to be exposed.

88. (Currently Amended) The apparatus of claim 87, wherein the separate areas are ~~predominantly~~ <u>substantially</u> non-overlapping.

89. (Previously Presented) The apparatus of claim 87, wherein a substantial portion of the separate areas are exposed simultaneously.

90. (Previously Presented) The apparatus of claim 86, wherein the emissions from the radiation source cells are selected from the group consisting of optical, Deep Ultra Violet, electron, and X-ray.

91. (Previously Presented) A lithography pattern generation device comprising:

an array of cells arranged in row and columns, the array being formed on a substrate, each cell being individually controlled to permit passage of charged particles from an external source; and

control logic integrated with the substrate for individually controlling each cell;

wherein each cell comprises an aperture for passage of charged particles onto a surface to be exposed.

92. (Currently Amended) The apparatus of claim 91, wherein ~~the cells expose~~ each cell exposes separate areas of the surface to be exposed.

93. (Currently Amended) The apparatus of claim 92, wherein the separate areas are ~~predominantly~~ substantially non-overlapping.

94. (Previously Presented) The apparatus of claim 92, wherein a substantial portion of the separate areas are exposed simultaneously.

95. (Previously Presented) The apparatus of claim 91, wherein the charged particles are selected from the group consisting of electrons and protons.

96. (Previously Presented) The apparatus of claim 91, further comprising a demagnifying lens.

97. (Previously Presented) A lithography pattern generation device comprising a plurality of exposure cells formed on a substrate where the exposure cells are controlled by control circuitry integrated on the substrate.

98. (Previously Presented) The apparatus of claim 97, wherein each exposure cell is selected from the group consisting of a radiation source cell and a shuttered cell.

99. (Currently Amended) The apparatus of claim 97, wherein ~~the~~ each exposure ~~cells expose~~ cell exposes separate areas of a surface to be exposed.

100. (Currently Amended) The apparatus of claim 99, wherein the separate areas are ~~predominantly~~ substantially non-overlapping.

101. (Previously Presented) The apparatus of claim 99, wherein a substantial portion of the separate areas are exposed simultaneously.

102. (Currently Amended) An apparatus for forming a patterned layer during manufacture of an integrated circuit, comprising:

a plurality of exposure elements; and

means for selectively irradiating with at least one type of radiant energy portions of a surface of a layer by electronically controlling individually each of the exposure elements.

103. (Previously Presented) The apparatus of claim 102, wherein the at least one type of radiant energy is selected from the group consisting of optical, Deep Ultra Violet, X-ray, E-beam, and particle beam.

104. (Previously Presented) The apparatus of claim 102, wherein the exposure elements are miniature sources of at

least one of the following types of radiant energy: X-ray, Deep Ultra Violet, and E-beam.

105. (Previously Presented) The apparatus of claim 102, wherein the exposure elements control passage of radiant energy from an external source.

106. (Previously Presented) The apparatus of claim 105, wherein the exposure elements control passage of radiant energy from an external source using at least one of the following mechanisms: electromagnetic deflection, electrostatic deflection and mechanical shuttering.

107. (Previously Presented) The apparatus of claim 102, comprising means for separately focusing radiant energy emitted from each of multiple different exposure elements.

108. (Previously Presented) The apparatus of claim 102, comprising means for:

ceasing irradiating the surface;

shifting the exposure elements with respect to the surface; and

resuming irradiating the surface.

109. (Previously Presented) The apparatus of claim 86, further comprising at least one stress-controlled dielectric layer.

110. (Currently Amended) The apparatus of claim 109, wherein the stress of the at least one stress-controlled dielectric layer is less <u>than</u> about 8 x 10^8 dynes/cm^2.

111. (Previously Presented) The apparatus of claim 86, further comprising at least one elastic dielectric layer.

112. (Previously Presented) The apparatus of claim 111, wherein the stress of the at least one elastic dielectric layer is less than about 8 x 10^8 dynes/cm^2.

113. (Previously Presented) The apparatus of claim 91, further comprising at least one stress-controlled dielectric layer.

114. (Currently Amended) The apparatus of claim 113, wherein the stress of the at least one stress-controlled dielectric layer is less <u>than</u> about 8 x 10^8 dynes/cm^2.

115. (Previously Presented) The apparatus of claim 91, further comprising at least one elastic dielectric layer.

116. (Previously Presented) The apparatus of claim 115, wherein the stress of the at least one elastic dielectric layer is less than about 8 x 10^8 dynes/cm^2.

117. (Previously Presented) The apparatus of claim 102, further comprising at least one stress-controlled dielectric layer.

118. (Currently Amended) The apparatus of claim 117, wherein the stress of the at least one stress-controlled dielectric layer is less <u>than</u> about 8 x 10^8 dynes/cm^2.

119. (Previously Presented) The apparatus of claim 102, further comprising at least one elastic dielectric layer.

120. (Previously Presented) The apparatus of claim 119, wherein the stress of the at least one elastic dielectric layer is less than about 8 x 10^8 dynes/cm^2.

121. (Previously Presented) A semiconductor processing lithography apparatus for maskless pattern generation comprising:

an array of radiation source cells arranged in rows and columns, the array being formed on a substrate;

a stress-controlled dielectric layer formed on the substrate; and

control logic integrated with the substrate for individually controlling each cell, wherein each cell comprises:

an exposure source; and

an aperture through which the exposure source emissions pass onto a surface to be exposed.

122. (Currently Amended) The apparatus of claim 121, wherein ~~the~~ each radiation source ~~cells expose~~ cell exposes separate areas of the surface to be exposed.

123. (Currently Amended) The apparatus of claim 122, wherein the separate areas are ~~predominantly~~ substantially non-overlapping.

124. (Previously Presented) The apparatus of claim 122, wherein a substantial portion of the separate areas are exposed simultaneously.

125. (Previously Presented) The apparatus of claim 121, wherein the emissions from the radiation source cells are selected from the group consisting of optical, Deep Ultra Violet, electron, and X-ray.

126. (Currently Amended) The apparatus of claim 121, wherein the stress of the at least one stress-controlled dielectric layer is less than about 8×10^8 dynes/cm^2.

127. (Previously Presented) The apparatus of claim 121, further comprising at least one elastic dielectric layer.

128. (Previously Presented) The apparatus of claim 127, wherein the stress of the at least one elastic dielectric layer is less than about 8×10^8 dynes/cm^2.

129. (Previously Presented) A lithography pattern generation device comprising:

an array of cells arranged in row and columns, the array being formed on a substrate, each cell being individually controlled to permit passage of charged particles from an external source;

a stress-controlled dielectric layer formed on the substrate; and

control logic integrated with the substrate for individually controlling each cell;

wherein each cell comprises an aperture for passage of charged particles onto a surface to be exposed.

130. (Currently Amended) The apparatus of claim 129 wherein ~~the cells expose~~ each cell exposes separate areas of the surface to be exposed.

131. (Currently Amended) The apparatus of claim 130, wherein the separate areas are ~~predominantly~~ substantially non-overlapping.

132. (Previously Presented) The apparatus of claim 130, wherein a substantial portion of the separate areas are exposed simultaneously.

133. (Previously Presented) The apparatus of claim 129, wherein the charged particles are selected from the group consisting of electrons and protons.

134. (Previously Presented) The apparatus of claim 129, further comprising a demagnifying lens.

135. (Currently Amended) The apparatus of claim 129, wherein the stress of the at least one stress-controlled dielectric layer is less than about 8 x 10^8 dynes/cm^2.

136. (Previously Presented) The apparatus of claim 129, further comprising at least one elastic dielectric layer.

137. (Previously Presented) The apparatus of claim 136, wherein the stress of the at least one elastic dielectric layer is less than about 8 x 10^8 dynes/cm^2.

138. (Currently Amended) An apparatus for forming a patterned layer during manufacture of an integrated circuit, comprising:

a plurality of exposure elements formed on a substrate;

a stress-controlled dielectric layer formed on the substrate; and

means for selectively irradiating with at least one type of radiant energy portions of a surface of a layer by electronically controlling <u>individually each of</u> the exposure elements.

139. (Previously Presented) The apparatus of claim 138, wherein the at least one type of radiant energy is selected from the group consisting of optical, Deep Ultra Violet, X-ray, E-beam, and particle beam.

140. (Previously Presented) The apparatus of claim 138, wherein the exposure elements are miniature sources of at least one of the following types of radiant energy: X-ray, Deep Ultra Violet, and E-beam.

141. (Previously Presented) The apparatus of claim 138, wherein the exposure elements control passage of radiant energy from an external source.

142. (Previously Presented) The apparatus of claim 141, wherein the exposure elements control passage of radiant energy from an external source using at least one of the following mechanisms: electromagnetic deflection, electrostatic deflection and mechanical shuttering.

143. (Previously Presented) The apparatus of claim 138, comprising means for separately focusing radiant energy emitted from each of multiple different exposure elements.

144. (Previously Presented) The apparatus of claim 138, comprising means for:

ceasing irradiating the surface;

shifting the exposure elements with respect to the surface; and

resuming irradiating the surface.

145. (Currently Amended) The apparatus of claim 138, wherein the stress of the at least one stress-controlled dielectric layer is less than about 8 x 10^8 dynes/cm^2.

146. (Previously Presented) The apparatus of claim 138, further comprising at least one elastic dielectric layer.

147. (Previously Presented) The apparatus of claim 146, wherein the stress of the at least one elastic dielectric layer is less than about 8×10^8 dynes/cm^2.

148. (New) The method of claim 77, wherein the plurality of exposure elements includes at least one million elements.

149. (New) The apparatus of claim 86, wherein the array of radiation source cells includes at least one million cells.

150. (New) The apparatus of claim 110, wherein the stress is tensile.

151. (New) The apparatus of claim 112, wherein the stress is tensile.

152. (New) The apparatus of claim 109, wherein the stress of the at least one stress-controlled dielectric layer is 2 to 100 times less than the fracture strength of the at least one stress-controlled dielectric layer.

153. (New) The apparatus of claim 152, wherein the stress is tensile.

154. (New) The apparatus of claim 109, wherein the at least one stress-controlled dielectric layer is at least one of elastic and flexible.

155. (New) The apparatus of claim 109, wherein the at least one stress-controlled dielectric layer is capable of forming at least one of a flexible membrane and a free standing membrane.

156. (New) The apparatus of claim 109, wherein the at least one stress-controlled dielectric layer is selected from the group consisting of silicon dioxide and silicon nitride.

157. (New) The apparatus of claim 109, further comprising a plurality of interconnect conductors formed within the at least one stress-controlled dielectric layer.

158. (New) The apparatus of claim 109, wherein the at least one stress-controlled dielectric layer is formed by multiple RF energy sources.

159. (New) The apparatus of claim 109, wherein the at least one stress-controlled dielectric layer is formed at a temperature of about 400°C.

160. (New) The apparatus of claim 91, wherein the array of cells includes at least one million cells.

161. (New) The apparatus of claim 114, wherein the stress is tensile.

162. (New) The apparatus of claim 116, wherein the stress is tensile.

163. (New) The apparatus of claim 113, wherein the stress of the at least one stress-controlled dielectric layer is 2 to 100 times less than the fracture strength of the at least one stress-controlled dielectric layer.

164. (New) The apparatus of claim 163, wherein the stress is tensile.

165. (New) The apparatus of claim 113, wherein the at least one stress-controlled dielectric layer is at least one of elastic and flexible.

166. (New) The apparatus of claim 113, wherein the at least one stress-controlled dielectric layer is capable of

forming at least one of a flexible membrane and a free standing membrane.

167. (New) The apparatus of claim 113, wherein the at least one stress-controlled dielectric layer is selected from the group consisting of silicon dioxide and silicon nitride.

168. (New) The apparatus of claim 113, further comprising a plurality of interconnect conductors formed within the at least one stress-controlled dielectric layer.

169. (New) The apparatus of claim 113, wherein the at least one stress-controlled dielectric layer is formed by multiple RF energy sources.

170. (New) The apparatus of claim 113, wherein the at least one stress-controlled dielectric layer is formed at a temperature of about 400°C.

171. (New) The apparatus of claim 97, wherein the plurality of exposure cells includes at least one million cells.

172. (New) The apparatus of claim 97, further comprising at least one stress-controlled dielectric layer.

173. (New) The apparatus of claim 172, wherein the stress of the at least one stress-controlled dielectric layer is less than about 8 x 10^8 dynes/cm^2.

174. (New) The apparatus of claim 173, wherein the stress is tensile.

175. (New) The apparatus of claim 172, wherein the stress of the at least one stress-controlled dielectric layer is 2 to 100 times less than the fracture strength of the at least one stress-controlled dielectric layer.

176. (New) The apparatus of claim 175, wherein the stress is tensile.

177. (New) The apparatus of claim 172, wherein the at least one stress-controlled dielectric layer is at least one of elastic and flexible.

178. (New) The apparatus of claim 172, wherein the at least one stress-controlled dielectric layer is capable of forming at least one of a flexible membrane and a free standing membrane.

179. (New) The apparatus of claim 172, wherein the at least one stress-controlled dielectric layer is selected from the group consisting of silicon dioxide and silicon nitride.

180. (New) The apparatus of claim 172, further comprising a plurality of interconnect conductors formed within the at least one stress-controlled dielectric layer.

181. (New) The apparatus of claim 172, wherein the at least one stress-controlled dielectric layer is formed by multiple RF energy sources.

182. (New) The apparatus of claim 172, wherein the at least one stress-controlled dielectric layer is formed at a temperature of about 400°C.

183. (New) The apparatus of claim 102, wherein the plurality of exposure elements includes at least one million elements.

184. (New) The apparatus of claim 118, wherein the stress is tensile.

185. (New) The apparatus of claim 120, wherein the stress is tensile.

186. (New) The apparatus of claim 117, wherein the stress of the at least one stress-controlled dielectric layer is 2 to 100 times less than the fracture strength of the at least one stress-controlled dielectric layer.

187. (New) The apparatus of claim 186, wherein the stress is tensile.

188. (New) The apparatus of claim 117, wherein the at least one stress-controlled dielectric layer is at least one of elastic and flexible.

189. (New) The apparatus of claim 117, wherein the at least one stress-controlled dielectric layer is capable of forming at least one of a flexible membrane and a free standing membrane.

190. (New) The apparatus of claim 117, wherein the at least one stress-controlled dielectric layer is selected from the group consisting of silicon dioxide and silicon nitride.

191. (New) The apparatus of claim 117, further comprising a plurality of interconnect conductors formed within the at least one stress-controlled dielectric layer.

192. (New) The apparatus of claim 117, wherein the at least one stress-controlled dielectric layer is formed by multiple RF energy sources.

193. (New) The apparatus of claim 117, wherein the at least one stress-controlled dielectric layer is formed at a temperature of about 400°C.

194. (New) The apparatus of claim 121, wherein the array of radiation source cells includes at least one million cells.

195. (New) The apparatus of claim 126, wherein the stress is tensile.

196. (New) The apparatus of claim 128, wherein the stress is tensile.

197. (New) The apparatus of claim 121, wherein the stress of the at least one stress-controlled dielectric layer is 2 to 100 times less than the fracture strength of the at least one stress-controlled dielectric layer.

198. (New) The apparatus of claim 197, wherein the stress is tensile.

199. (New) The apparatus of claim 121, wherein the at least one stress-controlled dielectric layer is at least one of elastic and flexible.

200. (New) The apparatus of claim 121, wherein the at least one stress-controlled dielectric layer is capable of forming at least one of a flexible membrane and a free standing membrane.

201. (New) The apparatus of claim 121, wherein the at least one stress-controlled dielectric layer is selected from the group consisting of silicon dioxide and silicon nitride.

202. (New) The apparatus of claim 121, further comprising a plurality of interconnect conductors formed within the at least one stress-controlled dielectric layer.

203. (New) The apparatus of claim 121, wherein the at least one stress-controlled dielectric layer is formed by multiple RF energy sources.

204. (New) The apparatus of claim 121, wherein the at least one stress-controlled dielectric layer is formed at a temperature of about 400°C.

205. (New) The apparatus of claim 129, wherein the array of cells includes at least one million cells.

206. (New) The apparatus of claim 135, wherein the stress is tensile.

207. (New) The apparatus of claim 137, wherein the stress is tensile.

208. (New) The apparatus of claim 129, wherein the stress of the at least one stress-controlled dielectric layer is 2 to 100 times less than the fracture strength of the at least one stress-controlled dielectric layer.

209. (New) The apparatus of claim 208, wherein the stress is tensile.

210. (New) The apparatus of claim 129, wherein the at least one stress-controlled dielectric layer is at least one of elastic and flexible.

211. (New) The apparatus of claim 129, wherein the at least one stress-controlled dielectric layer is capable of forming at least one of a flexible membrane and a free standing membrane.

212. (New) The apparatus of claim 129, wherein the at least one stress-controlled dielectric layer is selected from the group consisting of silicon dioxide and silicon nitride.

213. (New) The apparatus of claim 129, further comprising a plurality of interconnect conductors formed within the at least one stress-controlled dielectric layer.

214. (New) The apparatus of claim 129, wherein the at least one stress-controlled dielectric layer is formed by multiple RF energy sources.

215. (New) The apparatus of claim 129, wherein the at least one stress-controlled dielectric layer is formed at a temperature of about 400°C.

216. (New) The apparatus of claim 138, wherein the plurality of exposure elements includes at least one million elements.

217. (New) The apparatus of claim 145, wherein the stress is tensile.

218. (New) The apparatus of claim 147, wherein the stress is tensile.

219. (New) The apparatus of claim 138, wherein the stress of the at least one stress-controlled dielectric layer is 2 to 100 times less than the fracture strength of the at least one stress-controlled dielectric layer.

220. (New) The apparatus of claim 219, wherein the stress is tensile.

221. (New) The apparatus of claim 138, wherein the at least one stress-controlled dielectric layer is at least one of elastic and flexible.

222. (New) The apparatus of claim 138, wherein the at least one stress-controlled dielectric layer is capable of forming at least one of a flexible membrane and a free standing membrane.

223. (New) The apparatus of claim 138, wherein the at least one stress-controlled dielectric layer is selected from the group consisting of silicon dioxide and silicon nitride.

224. (New) The apparatus of claim 138, further comprising a plurality of interconnect conductors formed within the at least one stress-controlled dielectric layer.

225. (New) The apparatus of claim 138, wherein the at least one stress-controlled dielectric layer is formed by multiple RF energy sources.

226. (New) The apparatus of claim 138, wherein the at least one stress-controlled dielectric layer is formed at a temperature of about 400°C.